

● General Description

It combines planar MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

● Features

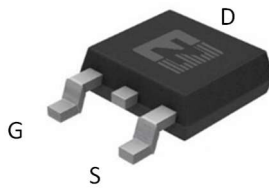
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low thermal resistance
- AEC-Q101 qualified

● Application

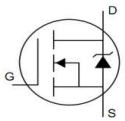
- Airbag
- Linear mode applications



● Product Summary



TO-252



$V_{DS}=75V$

$R_{DS(ON)}=28.7m\Omega$

$I_D=47A$



● Ordering Information

Part NO.	ZMPA160N08D
Marking	ZMP160N08
Packing information	REEL TAPE
Basic ordering unit (pcs)	2500

● Absolute Maximum Ratings ($T_A=25^\circ C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Drain-source voltage	V_{DS}	$25^\circ C \leq T_J \leq 175^\circ C$	-	75	V
Gate-source voltage ^①	V_{GS}	DC; $-55^\circ C \leq T_J \leq 175^\circ C$	-20	20	V
Continuous drain current	I_D	$V_{GS}=10V, T_C=25^\circ C$	-	47	A
	I_D	$V_{GS}=10V, T_C=75^\circ C$	-	39	A
	I_D	$V_{GS}=10V, T_C=100^\circ C$	-	34	A
Pulsed drain current	I_{DM}	Pulsed; $t_p \leq 10 \mu s; T_C = 25^\circ C$;	-	188	A
Diode continuous current	I_S	$V_{GS}=0V, T_C=25^\circ C$	-	47	A
Diode pulse current	$I_{S,pulse}$	Pulsed; $t_p \leq 10 \mu s; T_C = 25^\circ C$;	-	188	A
Total power dissipation	P_D	$V_{GS} > 6V, T_C=25^\circ C$	-	205	W
Total power dissipation	P_D	$V_{GS} > 6V, T_A=25^\circ C$	-	2.4	W
Operating junction temperature	T_J		-55	175	$^\circ C$
Storage temperature	T_{STG}		-55	175	$^\circ C$
Single pulse avalanche energy	E_{AS}	$L=0.5mH, V_{GS}=10V, R_g=25\Omega$	-	333	mJ

ESD level (HBM)		CLASS 2
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● Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	0.73	°C/W
Thermal resistance, junction - ambient	$R_{thJA}^{②}$	-	-	62	°C/W
Soldering temperature	T_{sold}	-	-	260	°C

● Electronic Characteristics ($T_j=25^{\circ}\text{C}$, unless otherwise specified)

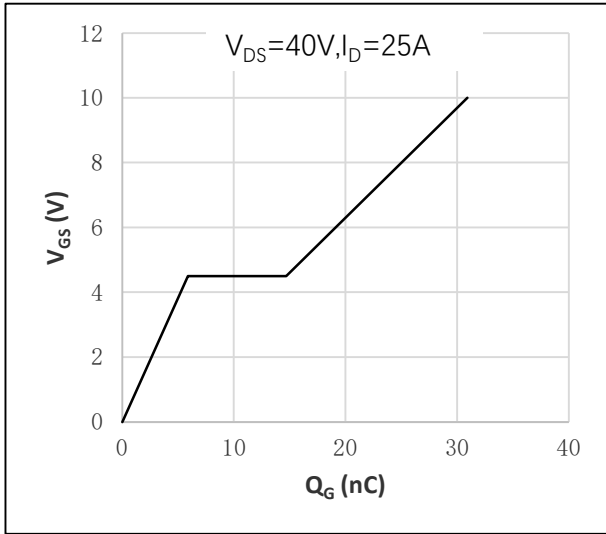
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A, T_j=25^{\circ}\text{C}$	75	-	-	V
		$V_{GS}=0V, I_D=1mA, T_j=-55^{\circ}\text{C}$	69.3	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A, T_j=25^{\circ}\text{C}$	1.2	2.1	2.5	V
		$V_{GS}=V_{DS}, I_D=1mA, T_j=-55^{\circ}\text{C}$	-	-	2.9	V
		$V_{GS}=V_{DS}, I_D=1mA, T_j=175^{\circ}\text{C}$	0.7	-	-	V
Drain-source leakage current	I_{DSS}	$V_{GS}=0V, V_{DS}=75V, T_j=25^{\circ}\text{C}$	-	-	1	μA
		$V_{GS}=0V, V_{DS}=75V, T_j=175^{\circ}\text{C}$	-	-	500	μA
Gate- source leakage current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Static drain-source on resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=25A, T_j=25^{\circ}\text{C}$	-	28.7	35.9	m Ω
		$V_{GS}=10V, I_D=25A, T_j=175^{\circ}\text{C}$	-	73	-	m Ω
		$V_{GS}=4.5V, I_D=15A, T_j=25^{\circ}\text{C}$		38.8	48.5	m Ω
Forward transconductance	g_{FS}	$V_{DS}=5V, I_{SD}=10A$	-	19	-	S
Diode forward voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=25A$	-	0.9	1.3	V

● Dynamic characteristics ($T_j=25^{\circ}\text{C}$, unless otherwise specified)

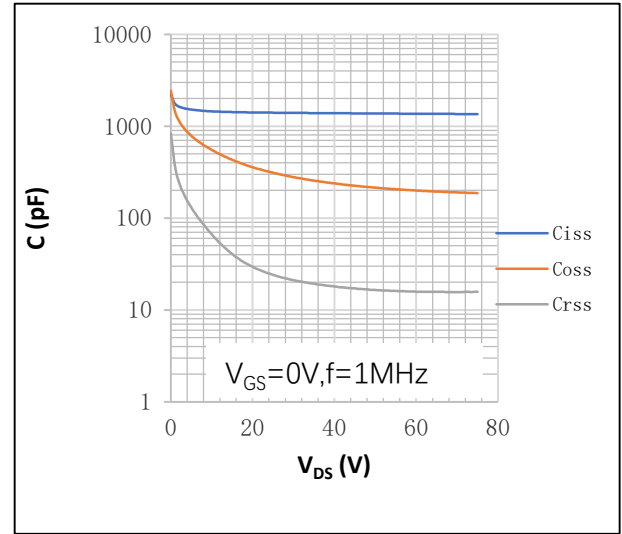
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1\text{MHz}, V_{DS}=40V, V_{GS}=0V$	-	1400	-	pF
Output capacitance	C_{oss}		-	278	-	pF
Reverse transfer capacitance	C_{rss}		-	21	-	pF
Gate resistance	R_g	$f=1\text{MHz}$	-	1.1	-	Ω
Total gate charge	Q_g	$V_{DD}=40V, I_D=25A, V_{GS}=10V$	-	30.9	-	nC
Total gate charge	$Q_{g(4.5V)}$		-	14.7	-	nC
Gate-source charge	Q_{gs}		-	5.9	-	nC
Gate-drain charge	Q_{gd}		-	8.8	-	nC

Turn-on delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=40V,$ $R_G=3.3\Omega, I_D=25A$	-	10	-	ns
Turn-on rise time	t_r		-	6	-	ns
Turn-off delay time	$t_{D(off)}$		-	25	-	ns
Turn-off fall time	t_f		-	5	-	ns
Reverse recovery time	t_{rr}	$V_{DD}=40V, di_s/dt = 100A/us,$ $I_s=25A$	-	46	-	ns
Reverse recovery charge	Q_{rr}		-	113	-	nC

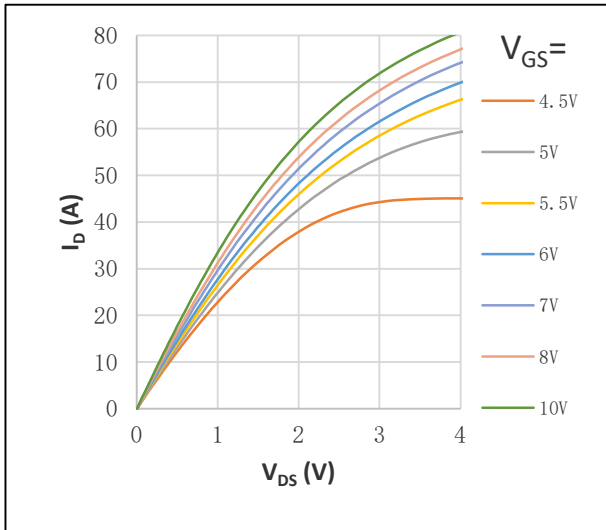
● Fig.1 Gate-source voltage as a function of gate charge; Typical values; $T_j=25^\circ\text{C}$



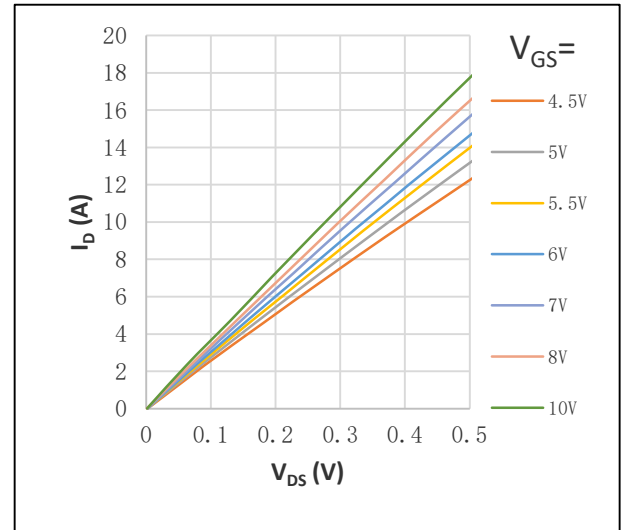
● Fig.2 Input, output and reverse transfer capacitances as a function of drain-source voltage; Typical values; $T_j=25^\circ\text{C}$



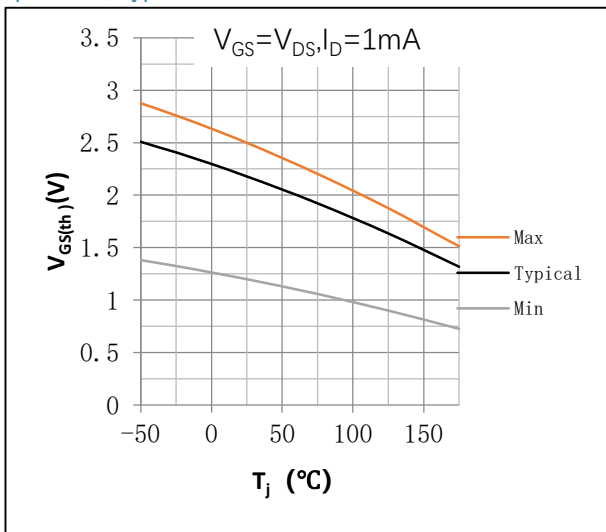
● Fig.3 Output characteristics: drain current as a function of drain-source voltage; Typical values; $T_j=25^\circ\text{C}$



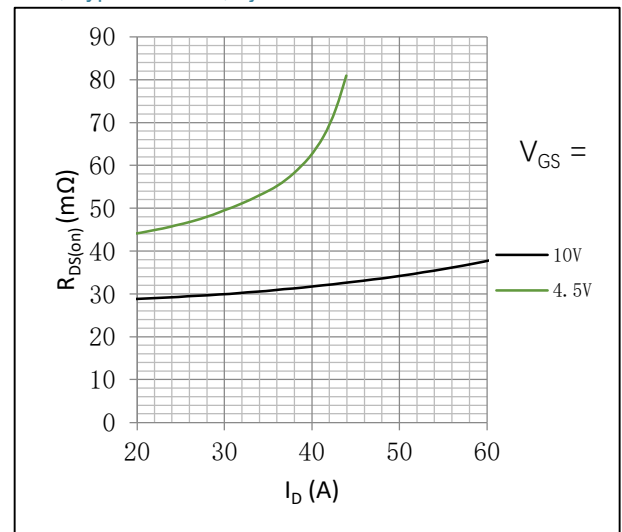
● Fig.4 Output characteristics: drain current as a function of drain-source voltage; Typical values: Expanded curve; $T_j=25^\circ\text{C}$



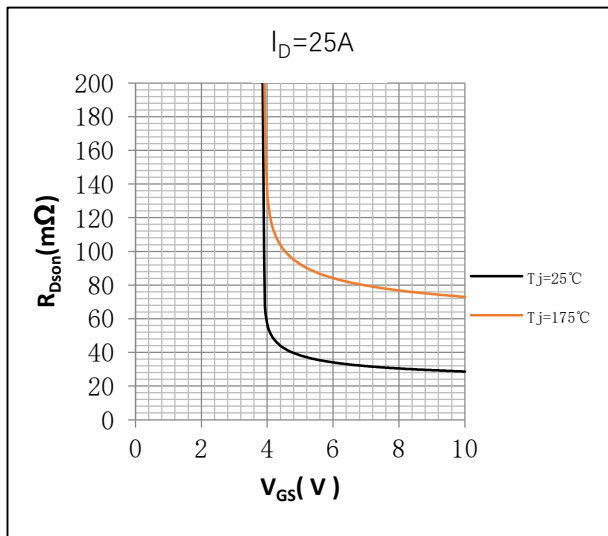
● Fig.5 Gate-source threshold voltage as a function of junction temperature; Typical/Min/Max values



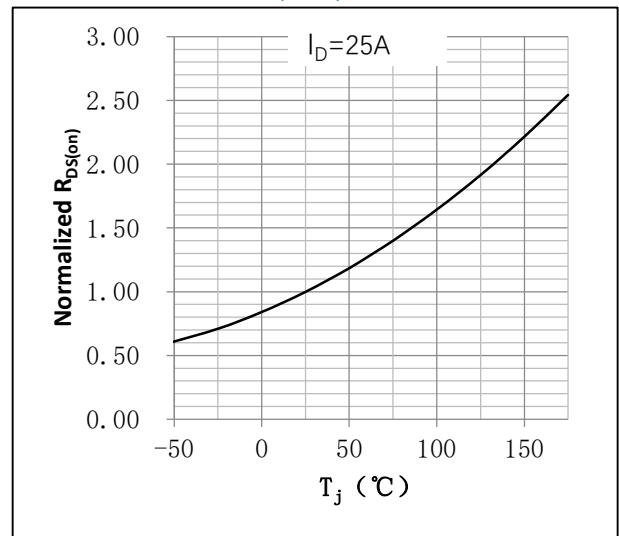
● Fig.6 Drain-source on-state resistance as a function of drain current; Typical values; $T_j=25^\circ\text{C}$



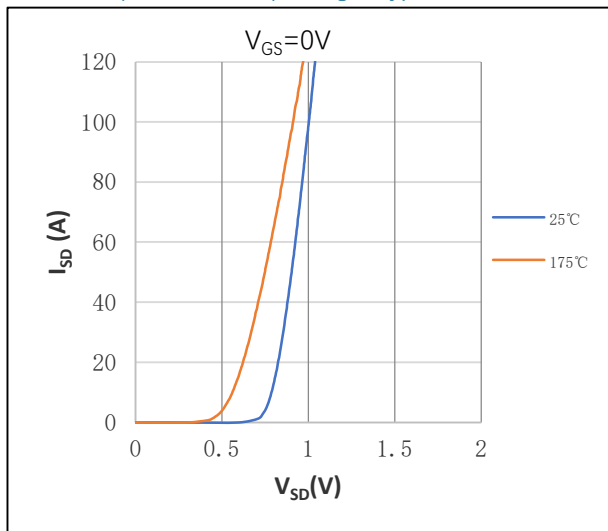
● Fig.7 Drain-source on-state resistance as a function of gate-source voltage; Typical values



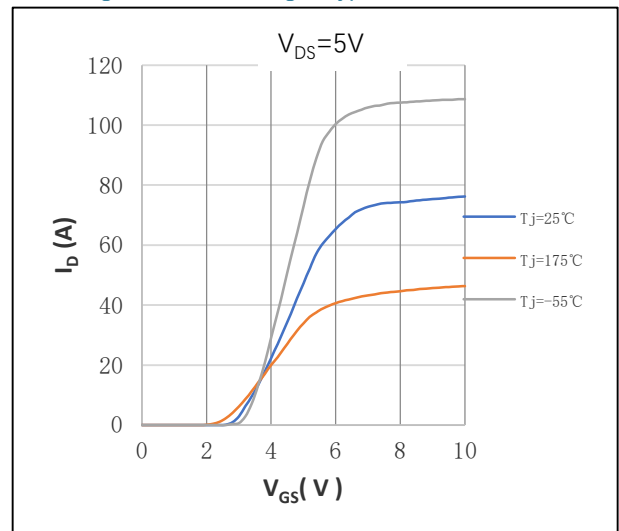
● Fig.8 Normalized drain-source on-state resistance factor as a function of junction temperature; Typical values Normalized On-Resistance= $R_{DS(on)}/R_{DS(on)}(25^{\circ}\text{C})$



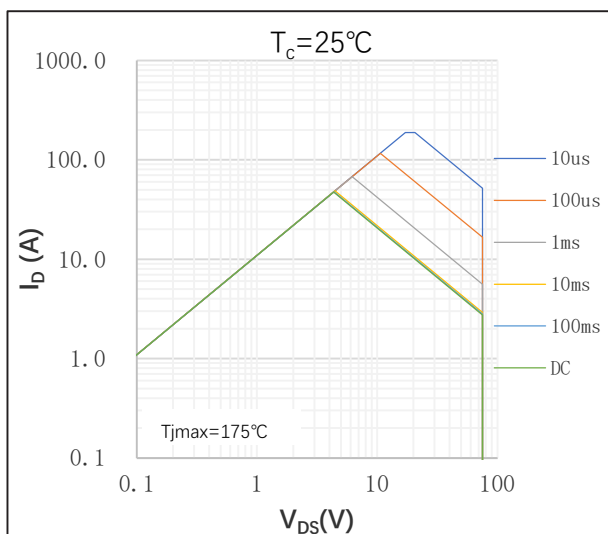
● Figure 9. Source (diode forward) current as a function of source-drain (diode forward) voltage; Typical values



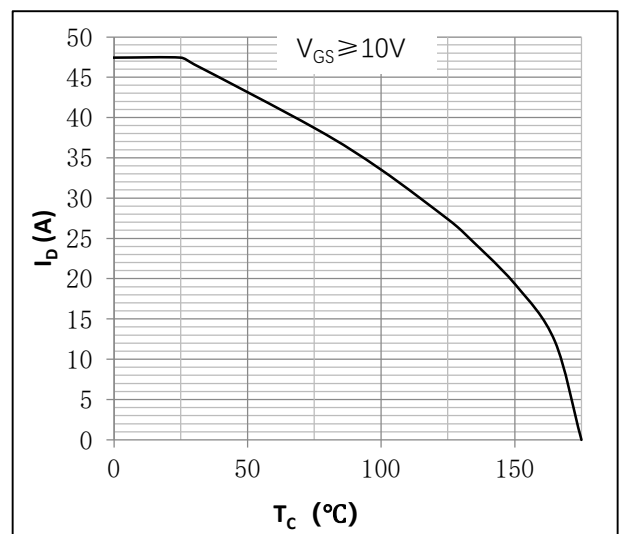
● Figure 10. Transfer characteristics: drain current as a function of gate-source voltage; Typical values



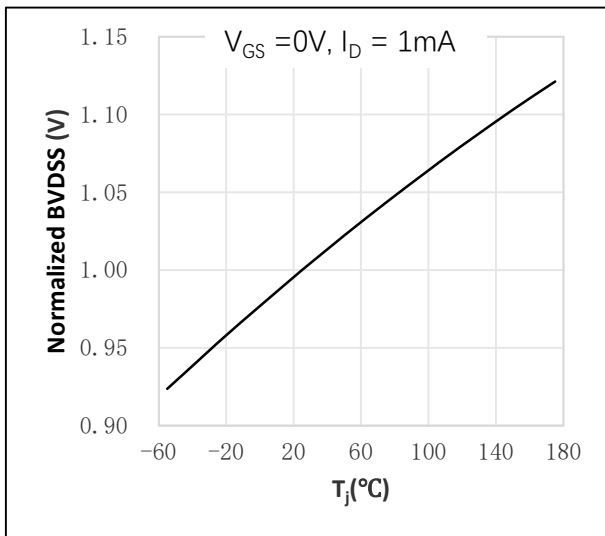
● Fig.11 Safe operating area: continuous and peak drain currents as a function of drain-source voltage; Calculative values



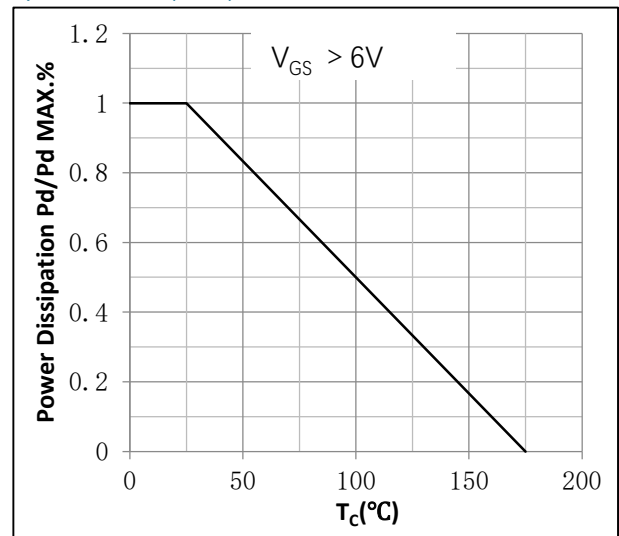
● Fig.12 Continuous drain current as a function of case temperature³; Calculative values



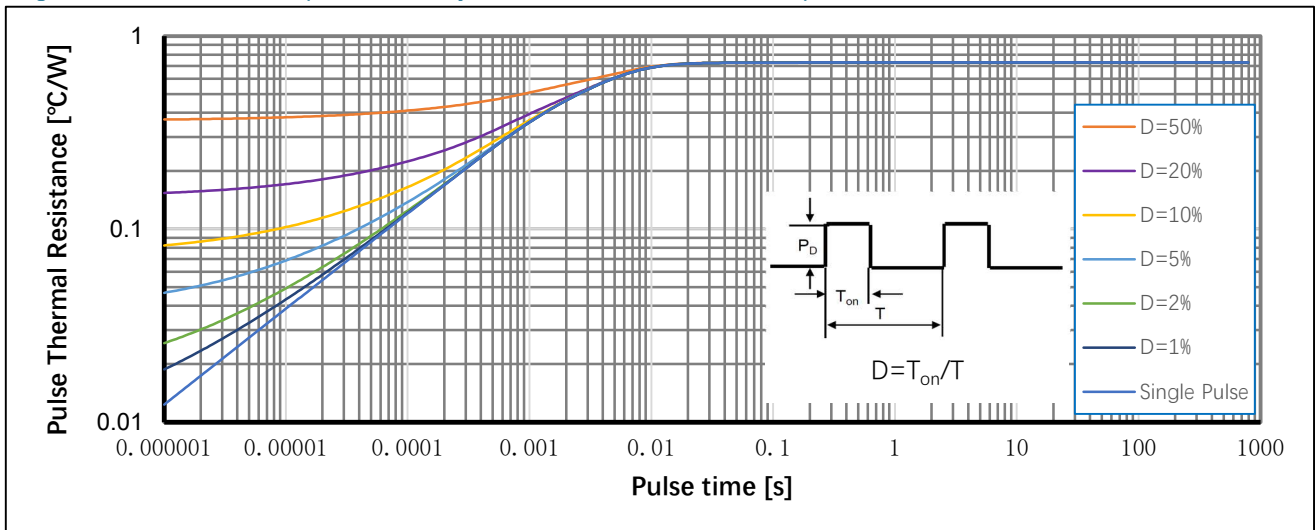
● Fig.13 Drain-source breakdown voltage as a function of junction temperature; Min values



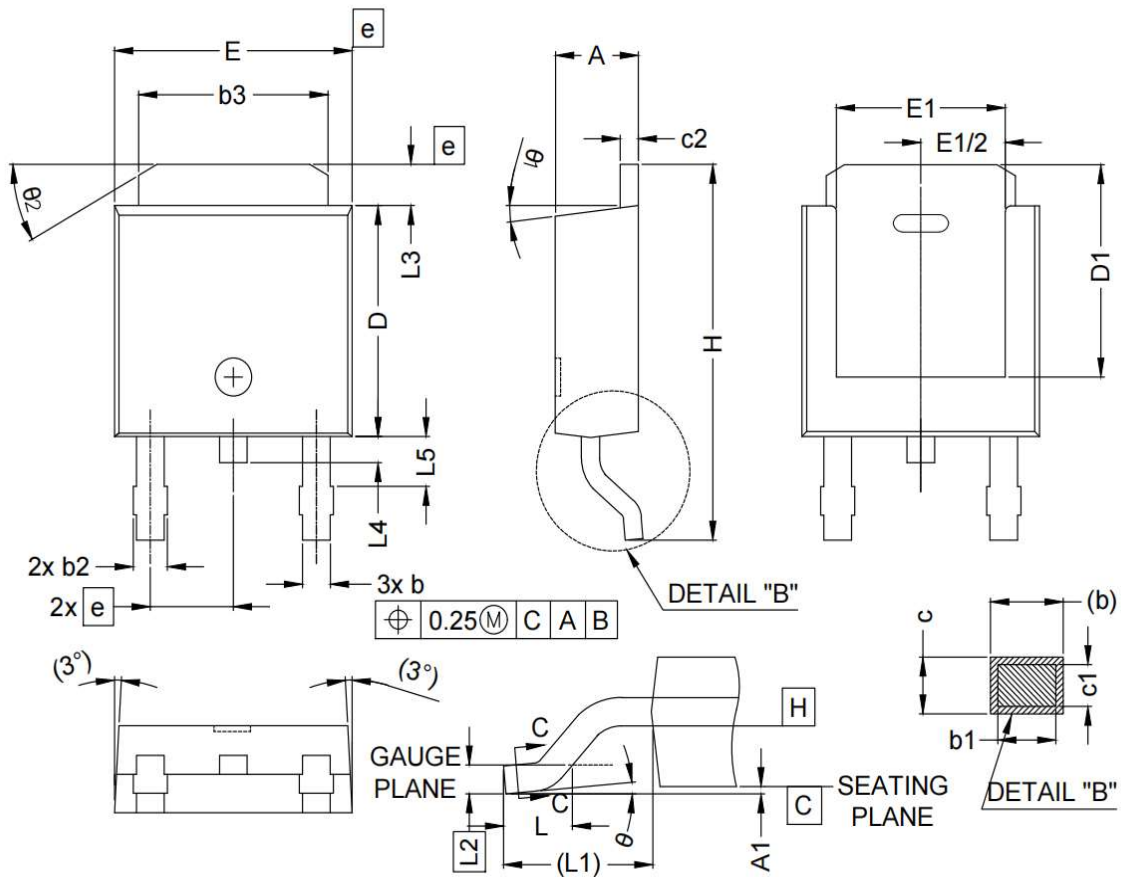
● Fig.14 Normalized total power dissipation as a function of case temperature; Calculative values Normalized Power Dissipation $= P_d / P_d(25^\circ C)$



● Fig.15 Transient thermal impedance from junction to case as a function of pulse duration; max values



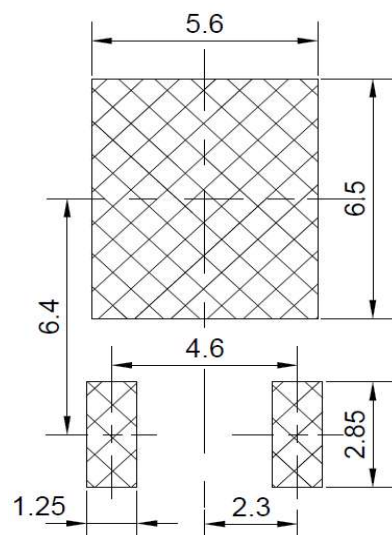
● Package Outline



NOTE ; 1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.
 2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
 3.0 HEAT SINK SIDE FLASH IS MAX. 0.8mm.
 4.0 RADIUS ON TERMINAL IS OPTIONAL.

SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.
A	2.18	2.39	E	6.35	6.73	θ1	0°	15°
A1	-	0.13	E1	4.32	-	θ2	25°	35°
b	0.65	0.89	e	2.29 BSC				
b1	0.64	0.79	H	9.94	10.34			
b2	0.76	1.13	L	1.50	1.78			
b3	4.95	5.46	L1	2.74 REF				
c	0.46	0.61	L2	0.51 BSC				
c1	0.41	0.56	L3	0.89	1.27			
c2	0.46	0.60	L4	-	1.02			
D	5.97	6.22	L5	1.14	1.49			
D1	5.21	-	θ	0°	10°			

Land Pattern (Only for Reference)



● Note

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC, the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=10V$.

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● Revision History

Version	Date	Change
Preliminary	2026/7/21	New